Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method of fabricating a flash memory, comprising:
sequentially forming a tunneling dielectric layer, a conductive layer and a mask layer on a substrate;
patterning the tunneling dielectric layer, the conductive layer and the mask layer into a strip structure;
performing an ion implantation step to form a buried drain region in the substrate between the strips;
patterning the strip structure to form a control gate structure, in which the patterned conductive layer is further patterned into a floating gate;
forming an insulation layer on a sidewall of the floating gate structure, the insulation layer having a top surface lower than a top surface of the floating gate such that a part of a sidewall of the floating gate is exposed;
removing the patterned mask layer;
forming a gate dielectric layer on the top surface and the exposed sidewall of the floating gate; and
forming a control gate on the gate dielectric layer.

[c2] 2. The method according to Claim 1, wherein the step of forming the insulation layer further comprises:
forming an insulation layer on the substrate to cover the

floating gate structures and to fill space between the floating gate structures;

removing a part of the insulation layer that covers the floating gate structures to expose the patterned mask layer; and

removing a part of the remaining insulation layer until the top surface of the insulation layer is between a top surface and a bottom surface of the floating gate.

[c3] 3. The method according to Claim 2, further comprising forming the insulation layer with silicon oxide, silicon nitride, or spin-on glass.

[c4] 4. The method according to Claim 2, further comprising using high-density plasma chemical vapor deposition for forming the insulation layer.

[c5] 5. The method according to Claim 4, further comprising using tetra-ethyl-oxy-silicate and ozone.

[c6] 6. The method according to Claim 2, further comprising using chemical mechanical or etch back to remove part of the insulation layer.

[c7] 7. The method according to Claim 2, further comprising using etch back to remove the remaining insulation layer.

[c8] 8. The method according to Claim 1, further comprising forming the mask layer with silicon oxide or silicon nitride.

[c9] 9. The method according to Claim 8, further comprising using wet etching to remove the mask layer.

[c10] 10. The method according to Claim 8, further comprising using phosphoric acid as etchant to remove the mask layer when the mask layer is made of silicon nitride.

[c11] 11. A method of fabricating a flash memory, comprising:
forming a tunneling dielectric layer and a floating gate on a substrate;
forming a buried drain region in the substrate between the floating gates;
performing an ion implantation step to form a buried drain region in the substrate between the floating gates;
forming an insulation layer on a sidewall of the floating gate, the insulation layer having a top surface level between a top surface and a bottom surface of the floating gate;
forming a gate dielectric layer on the top surface and the exposed sidewall of the floating gate; and
forming a control gate on the gate dielectric layer.

[c12] 12. The method according to Claim 11, wherein the step

of forming the insulation layer further comprises:
forming an insulation layer on the substrate to cover the floating gate and to fill space between the floating gates;
removing a part of the insulation layer that covers the floating gate to expose the top surface of the floating gate; and
removing a part of the remaining insulation layer until the top surface of the insulation layer is between the top surface and the bottom surface of the floating gate.

[c13] 13. The method according to Claim 12, further comprising forming the insulation layer with silicon oxide.

[c14] 14. The method according to Claim 13, further comprising using high-density plasma chemical vapor deposition for forming the insulation layer.

[c15] 15. The method according to Claim 14, further comprising using tetra-ethyl-oxy-silicate and ozone.

[c16] 16. The method according to Claim 12, further comprising using chemical mechanical or etch back to remove the part of the insulation layer.

[c17] 17. The method according to Claim 1, further comprising a step of forming a mask on the floating gate when the part of the insulation layer formed subsequently is removed by chemical mechanical polishing; and a step of

removing the mask layer before forming the gate dielectric layer, wherein the mask layer is made of a material different from that of the insulation layer.

[c18] 18. The method according to Claim 18, further comprising using wet etching to remove the mask layer.

[c19] 19. The method according to Claim 12, further comprising using etch back to remove the part of the insulation layer.